Exhibit 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co. Ltd.	Case No. IPR2022-01427
Petitioner,	Patent No. 9,318,160
vs.	
Netlist, Inc.,	Case No. IPR2022-01428
Patent Owner.	Patent No. 8,787,060

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VIDEOCONFERENCE DEPOSITION OF ANDREW WOLFE, Ph.D.

Tuesday, June 27, 2023

Volume I (Pages 1 - 191)

Reported Remotely and Stenographically by:

JANIS JENNINGS, CSR No. 3942, CLR, CCRR

Job No. 5965315

DEPOSITION OF ANDREW WOLFE, Ph.D., appearing remotely, located in Santa Clara, California, taken on behalf of the Petitioner, beginning at 8:58 a.m., on Tuesday, June 27, 2023, sworn remotely by Janis Jennings, Certified Shorthand Reporter No. 3942, CCRR, located in the City of Walnut Creek, County of Contra Costa, State of California.

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I N D E X

E X H I B I T S

different bit values? 09:45
MR. CHANDLER: Objection. Form. 09:45
BY MS. ZHONG: 09:45
Q. For example, one is outputting 1, the other 09:45
is outputting 0, then the signal can't be 09:45
transmitted correctly, there is going to be 09:45
collision? 09:45
MR. CHANDLER: Objection. Form. 09:45
THE WITNESS: Again, that is not the actual 09:45
configuration of Riho, but that would be one of the 09:45
possible problems that could occur if you were to 09:45
try to connect D15 and D14 both to the same TSV and 09:45
allow them to output at the same time. But again -- 09:45
BY MS. ZHONG: 09:46
Q. What other problems -- okay. 09:46
What other problems would there be if you 09:46
connected D15 and D14 to the same TSV and allow them 09:46
to output data simultaneously? 09:46
MR. CHANDLER: Objection. I don't think he 09:46
finished his previous answer. 09:46
THE WITNESS: I did. 09:46
But one of the problems, there could be 09:46
speed-related problems. There could be 09:46
current-related problems. There could be damage to 09:46
circuits. Again, that's not the way Riho is 09:46

designed. So -- 09:46
BY MS. ZHONG:
Q. I understand. 09:46
When you say there could be "speed-related 09:46
problems," what problems are you referring to in 09:46
specific? 09:46
A. Again, that's not the way Riho was designed 09:46
and it's not a design that makes any sense. So if 09:46
one were to do it in practice, one would make other 09:46
changes as well to make it work. 09:47
But Riho treats D14 and D15 as two parts of 09:47
the same data work. Each one supplies 32 bits. 09:47
They are operated at the same time and each of one 09:47
requires 32 wires to communicate those 32 bits. 09:47
That's its mode of operation. 09:47
If you were to redesign it, you would have 09:47
to make some substantial changes to -- to change the 09:47
way that it operates to make sure that it operates 09:47
correctly and effectively. You couldn't just only 09:47
connect D14 and D15 to the same set of vias without 09:47
any other changes and expect it to operate 09:47
correctly. 09:47
Q. What if D14 and D15 belonged to two 09:47
different ranks, so they don't operate 09:48
simultaneously but belong, say, for example, to the 09:48

same logic rank? Can you do that? 09:48
MR. CHANDLER: Objection. Form. 09:48
THE WITNESS: I don't know. That's not -- 09:48
BY MS. ZHONG:
Q. Not really -- okay. Not can you do that, 09:48
but would a POSITA do that? 09:48
MR. CHANDLER: Objection. Form. 09:48
DEPOSITION REPORTER: Can you repeat your 09:48
question, please. 09:48
BY MS. ZHONG: 09:48
Q. What if D14 and D15 belonged to two 09:48
different ranks so they don't operate 09:48
simultaneously, would a POSITA make such a 09:48
configuration? 09:48
A. I don't think they would start with Riho to 09:48
do that. Again, there are lots of different kinds 09:49
of memory configurations that a POSITA knows how to 09:49
do and can make work properly. 09:49
I would have to look at a complete design to 09:49
understand what the impact would be of making that 09:49
kind of a change, but you wouldn't make that change 09:49
without making other changes as well. 09:49
Q. What other change would you make? 09:49
MR. CHANDLER: Objection. Form. 09:49
Incomplete. 09:49

THE WITNESS: I don't know. I would have to 09:49
think it through. 09:49
Again, I'm not going to try to design a 09:49
complete working memory system based on a 09:49
hypothetical sitting here today. But you would make 09:49
sure you had the appropriate control signals and the 09:49
appropriate bus switching and you would analyze the 09:49
timing and the electrical operation and you would 09:49
make it work. 09:49
BY MS. ZHONG: 09:49
Q. Would that involve substantial redesign or 09:49
just a little bit of work? 09:49
MR. CHANDLER: Objection. Form. 09:50
THE WITNESS: I don't know until I try it. 09:50
Again, I wouldn't start from Riho and make that 09:50
particular change because it really doesn't seem to 09:50
be something that Riho was contemplating. There are 09:50
lots of other modifications one can make to Riho, 09:50
but making D14 and D15 not operate simultaneously 09:50
would not be one that I would use Riho as a starting 09:50
point for. 09:50
BY MS. ZHONG: 09:50
Q. And you said you would not start with Riho. 09:50
Is it because in Riho, D15, D14, et cetera, belong 09:50
to the same rank and they are intended to operate 09:51

simultaneously? 09:51
MR. CHANDLER: Objection. Form. 09:51
THE WITNESS: In Riho's preferred 09:51
embodiment, D0 through D7 are part of the same rank 09:51
and D8 through D15 are part of a second rank, and 09:51
that's the way his preferred embodiment works. 09:51
BY MS. ZHONG: 09:51
Q. Okay. What's the significance of belonging 09:51
to the same rank? 09:51
A. I'm not sure I understand the question. 09:51
Q. You said in Riho's preferred embodiment, 09:51
D0 through D7 are part of the same rank, and D8 09:51
through D15 are part of the second rank, and that's 09:51
the way his preferred embodiment works. 09:51
So my question to you is: What is 09:52
significant that D8 -- for example, D8 through D15 09:52
are part of one rank and D0 through D7 belongs to 09:52
another rank? 09:52
A. Again, I don't understand the question. I 09:52
was answering your previous question about how the 09:52
ranks were organized. 09:52
Q. Okay. So if the dies belong to the same 09:52
rank, what would happen if a read command is sent to 09:52
the stack array? Does that mean all eight of the 09:52
dies in the same rank is going to output data 09:52

simultaneously? 09:52
MR. CHANDLER: Objection. Form. 09:52
THE WITNESS: In the Figure 5 embodiment of 09:52
Riho, if you issue a read operation, all of the DRAM 09:52
die in a single rank will send data to the logic LSI 09:53
chip simultaneously. 09:53
BY MS. ZHONG: 09:53
Q. Is that how DRAMs are supposed to operate, 09:53
all the dies in the rank is supposed to respond to a 09:53
read signal and operate output data simultaneously? 09:53
MR. CHANDLER: Objection. Form. 09:53
THE WITNESS: It depends on the particular 09:53
design. 09:53
BY MS. ZHONG: 09:53
Q. So there are ranks -- there are embodiments 09:53
in which the dies in a rank do not respond to a read 09:53
operation -- a read command and output data 09:53
simultaneously? 09:53
MR. CHANDLER: Objection. Form. 09:53
THE WITNESS: Conceptually one could build 09:53
a DRAM system where either the entirety of a rank 09:53
could respond or a portion of a rank could respond 09:54
depending on the size of the read request. There 09:54
are lots of different ways that one could build a 09:54
memory system. 09:54

BY MS. ZHONG: 09:54
Q. Okay. I thought a rank is a collection of 09:54
DRAMs that respond to a common memory command 09:54
simultaneously. That's not your understanding of 09:54
what rank is? 09:54
MR. CHANDLER: Objection. Form. 09:54
THE WITNESS: That is my understanding. 09:54
But I think in common usage, one would still call 09:54
something a rank if it had that capability but also 09:54
had the capability to do a partial read. 09:54
BY MS. ZHONG: 09:54
Q. Where does that definition come from? 09:54
MR. CHANDLER: Objection. Form as to the 09:54
question there. 09:55
THE WITNESS: I just think that's common 09:55
usage, right? If a -- if a rank can provide data 09:55
simultaneously from each DRAM chip, I don't think it 09:55
has to in every instance for a person of ordinary 09:55
skill to refer to it as a rank. 09:55
BY MS. ZHONG: 09:55
Q. So you think "rank" can refer to a set of 09:55
family devices that read or write less than a full 09:56
bit width of the memory module in response to 09:56
command signals? 09:56
MR. CHANDLER: Objection. Form. 09:56

THE WITNESS: I don't think that's quite 09:56
what I said. 09:56
BY MS. ZHONG: 09:56
Q. Okay. Then can you further explain what you 09:56
meant? 09:57
A. I think I gave a pretty clear explanation, 09:57
but I will try one more time. 09:57
A rank of memory in the way that we 09:57
ordinarily use that term is capable of providing an 09:57
output on a read from every memory die or every 09:57
memory element in the rank simultaneously, but we 09:57
would still in normal usage still call it a rank if 09:57
it also had the capability of only providing a 09:57
portion of the memory word. 09:57
Q. So what you are saying is half a rank is 09:57
still referred to a rank? 09:57
MR. CHANDLER: Objection. Form. 09:58
THE WITNESS: No. I think I gave a clear 09:58
explanation of what I was saying. 09:58
BY MS. ZHONG: 09:58
Q. Okay. Let me see if I understand it. 09:58
So let's say that 8 memory dies in a rank to 09:58
output 64 bits, which is the bit width of the memory 09:58
module, and if now only one of the die is outputting 09:58
8 of the bits, you are still saying that the -- that 09:58

single die constitutes the rank; is that right? 09:59
A. No. I didn't -- there are no memory modules 09:59
really that I can recall in this IPR at all. But 09:59
even in that case, that was not what my testimony 09:59
was. 09:59
Q. Okay. So let's say 8 dies are outputting 09:59
64 bits from the memory system. Okay? And if for 09:59
one of the operation, only 8 bits are output. How 09:59
many -- how many dies are there in the rank? Still 09:59
8 or only 1? 09:59
A. 8. If the 8 dies normally operate together 09:59
and output 64 bits, the fact that there is an 10:00
additional operation in which only one operates does 10:00
not make the 8s stop being a rank. 10:00
Q. You said it normally outputs 64 bits, but 10:00
what if there are no what you call the normal -- 10:00
each operation is of variable length -- 10:00
MR. CHANDLER: Objection. 10:00
BY MS. ZHONG: 10:00
Q. -- then what would be -- what would 10:00
constitute a rank? 10:00
MR. CHANDLER: Objection. Form. 10:00
THE WITNESS: I can't recall ever seeing 10:00
such a situation, so I don't know what a person of 10:00
ordinary skill would call it. I would have to look 10:00

at the details. 10:00
BY MS. ZHONG: 10:00
Q. So let's say in the read operation, 10:00
sometimes it's 16 bits, sometimes it's 32 bits, 10:00
sometimes it's 64 bits. How many dies would you say 10:00
would make up a rank if each of the die is by 8? 10:00
MR. CHANDLER: Objection. Form. 10:01
THE WITNESS: Again, I would have to look at 10:01
the particulars, the particular situation. You 10:01
know, it would really depend on how that particular 10:01
system was configured. 10:01
But ordinarily we would refer to the 10:01
complete set of die that can operate concurrently, 10:01
that can output at the exact same time in a single 10:01
data word as a rank, whether or not it's possible to 10:01
use a portion of the rank. 10:01
BY MS. ZHONG: 10:01
Q. So if two dies belong to the same physical 10:02
rank, would you connect them with a single TSV and 10:02
have them output data simultaneously? 10:02
MR. CHANDLER: Objection. Form. Incomplete 10:02
hypothetical. 10:02
THE WITNESS: These are Riho's dies? 10:02
BY MS. ZHONG: 10:02
Q. It doesn't have to be. 10:02

A. I'd have to look at the specifics. I think 10:02
it would generally be difficult to have two die both 10:02
output simultaneously to the same TSV and have it 10:02
operate correctly. 10:02
Q. Because of potential data collision? 10:02
A. There could be a data collision. There 10:03
could be an electrical problem. I mean, that's just 10:03
not the way a wire in a memory circuit normally 10:03
operates. In a memory circuit, a wire with TSV is 10:03
just a specific kind of a wire. In normal 10:03
operation, it is usually driven by one driver at a 10:03
time. 10:03
Q. Okay. When you say "TSV is just a wire," 10:03
by "wire" you're not really -- it doesn't really 10:03
have the same meaning as the wire in wire bonding, 10:03
does it? 10:03
A. What I said was that TSV is a kind of a 10:03
wire. A wire bond is -- 10:03
Q. Okay.
A. -- a kind of a wire. 10:03
Q. Okay. When you say "wire," what do you 10:03
mean? Just electrical, a conducting trace or like 10:03
conductor? 10:03
A. A metallic conductor. 10:03
Q. So when you use the word "wire," you mean 10:03

metallic conductor? 10:04
MR. CHANDLER: Objection. Form. 10:04
THE WITNESS: That would be most commonly. 10:04
Again, there can be different contexts, but most 10:04
commonly that is what I would mean. 10:04
BY MS. ZHONG: 10:04
Q. What if the two dies don't belong to the 10:04
same physical rank but belong to a logical rank, 10:04
can you connect them to the same wire? 10:04
A. I'm so out of context here that I can't even 10:04
answer your question. I don't know what dies we are 10:04
talking about. I don't know what definition you are 10:04
using for physical rank and logical rank. I'd have 10:04
to look at an actual block diagram or circuit. 10:04
Q. Okay. So by logical rank -- and you are 10:05
familiar with the concept of rank multiplication; 10:05
right? 10:05
(Clarification requested by Reporter.) 10:05
BY MS. ZHONG:
Q. Rank multiplication. 10:05
A. Yes. Although there are many varieties. 10:05
Q. Okay. So in rank multiplication, you are 10:05
presenting -- on a high level, you are presenting 10:05
two physical ranks of memory dies as a single rank 10:05
to the memory controller; is that right? 10:05